CSI 250 - Homework Set #3

A master-slave configuration of a D Flip Flop is sometimes called an edge-triggered flip-flop because its output changes along only one specific clock cycle change. In practice, often, the master is set to active when the clock is low and the slave is set to active when the clock is high such that the output of the whole system, Q, changes when the clock moves from low to high. This means that when the clock is low, inputs to the master flip-flop is "active" and when the clock is high, inputs to the slave flip-flop is active and the final Q output gets set. Use this configuration in the answers to the following questions. You can just draw a box labeled D-edge with a single input D, a clock input CLK and a single output Q. It will be assumed D-edge will be two D flip flops set up in the master-slave configuration as described above.

1. A circuit called CLK runs at 1 Hz. There is an input coming from an outside source called M. The M input changes once a second. Derive a circuit whose output is 1 if the last three inputs of M were "101" and 0 otherwise. Use edge-triggered flip-flops, the CLK, M and any number of AND, OR, NAND, NOR and NOT gates to derive your answer. This "detector" circuit is called A.

2. Complete the circuit for A given a 3-bit shift register. You may still use CLK, M, and any number of other gates to compute your results.

3. Describe a hazard or race condition.

4. A Master-Slave D Flip Flop is configured such that the output from the slave is passed to an inverter (NOT) and then passed as input to D input of the master. Describe how this configuration works. Discuss its behavior in relation to the clock input as well.