Architecture Review Sheet #1

Page numbers in Appendices

- Logic Gates and Truth Tables (p442-447)
- Algebraic manipulations and representations (p450)
- SOP (p453)
- MUX, DeMUX, Decoder, Encoder, PLA (461-471)
- Flip Flops (Focus on S-R), clock, master-slave (472-479)
- race conditions, glitches, hazards (474)
- Karnaugh maps (503-508)

Page numbers in Comer text

- Logic Gates and Diagrams (9-10, 12-14)
- Flip flops (15-17)
- Clocks (18)
- Demux (19)
- Binary Arithmetic (31)
- Hexadecimal (32-33)
- Signed Binary (37-39)
- Floating Point (p40-42)
- von Neumann (p47-49)

Other topics

- bus architectures (vs von Neumann) (bus-like is shown on p51)
- backward compatibility and levels of architecture (high level vs low

level)

- fixed point, range and precision

- conversions between arbitrary base (remainder and multiplication methods)