Computer Organization and Architecture, Exam #1 Review

- von Neumann, CPU, modern computers, buses (4–6)
- Upward/Backward Compatibility (6–7)
- Levels of Architecture (high vs. low) (7–11)
- Fixed point, range, precision, overflow (20–21)
- Converting between arbitrary base (22-29)
- Binary Representations (1s complement, 2s complement, excess) (30–33)
- Floating Point, IEEE format (35–48)
- Truth Tables (442-443)
- Logic Gates, Diagrams and Truth Tables (444–447)
- Algebraic manipulations and representations (450)
- SOP, POS, minterms, maxterms (453–456)
- MUX, DeMUX, Decoder, Encoder, PLA (461–471)
- SR Flip Flops, Clocked SR, timing diagrams (472–474)
- D flip flops, JK flip flops, T flip flops, master-slave (476–479)
- race conditions, glitches and hazards (474)
- State transition diagrams, state tables, reduction, assignment (479–482, 528–529)
- Karnaugh maps (503–508)