MAT 250 — Introduction to Computer Organization and Architecture, Fall 2004

Final Review Sheet (#3)

- See Review Sheet #1 and Review Sheet #2
- Memory - Chapter 7 p 243
  - Moore's Law p243
  - Memory size increase rates p243
  - Memory speed increase rates p243
  - Memory Hierarchy - Helps solve the memory "gap" p243
  - Registers, Cache, Main Memory, Secondary Stage (hard drive) p244
  - Relative amts used, costs, and rough access times p244
  - RAM - Random Access Memory p245
  - SRAM - flip-flops p245
  - DRAM - capacitors p245
  - Comparison of DRAM and SRAM p245
  - ROM, PROM (examples) p252
  - locality principle p254
  - temporal locality (definition and examples) p254
  - spatial locality (definition and examples) p254
  - Cache Memory - small but fast p254
  - What is kept in the Cache? Where is the Cache? p254
  - What are: hits, misses p257
  - Associative Mapped Cache - each slot can access any address p255
  - Associative Mapped Caches (diagram, purpose, advantages, disadvantages) p256
  - Associative Mapped Cache - (tag,blocks, words,valid bits, dirty bits) p256
  - Replacement Policies descriptions and examples (LRU, FIFO, LFU, random, optimal) p258
  - Direct Mapped Cache - each slot can access specific addresses p259
  - Direct Mapped Caches (diagram, purpose, advantages, disadvantages) p259
  - Cache Hit Ratio - definition, formula, importance p264
  - Effective Access Time - definition, formula, importance p264