MAT 250 — Introduction to Computer Organization and Architecture, Fall 2004

Review Sheet #1

- von Neumann, CPU of the von Neumann machine, modern computers, buses, pp 4 – 6
- Upward Compatibility, pp 6 – 7
- Levels of Architecture (high - low), pp 7 – 11
- Truth tables, pp 442 – 443
- Logic Gates, pp 444
- AND, OR, NAND, NOR, XOR diagrams, algebra and truth tables, pp 444 – 447
- Algebraic manipulations and representations, pp 450
- Sum of Products (SOP, minterms, POS, maxterms), pp 453 – 456
- MUX , DeMUX, Decoder, Encoders, PLAs, Ripple Adders, pp 461 – 471
- SR Flip-Flops with timing diagrams, pp 472 – 473
- Clocked SR with timing diagrams, pp 474
- Race conditions, glitches and hazards, pp 474
- Cycle time, cycle rate, and hertz computation, pp 475
- D flip flops, pp 476
- Master-slave configuration using D flip flops, pp 477
- JK flip flops and T flip flops, pp 477 – 479
- State transition diagrams, state tables, pp 479 – 482
- Karnaugh maps, pp 503 – 508
- State Reduction, pp 524 – 527
- State assignment, State assignments w/ K-maps, pp 528 – 529
- Fixed Point, range, precision, overflow, pp 20 – 21
- Converting between binary, octal, hexadecimal and decimal, pp 22 – 29
- Binary number representations (1s complement, 2s complement, excess), pp 30 – 33

- Adding binary, pp 29 – 30
- Floating point representation, pp 35 – 37
- Single precision, double precision, IEEE format, pp 45 – 48

Previous Homework

- Appendix A: 2, 3, 6, 8, 9, 12, 25, 29, 33
- Appendix B: 1, 4, 11
- Chapter 2: 1, 2, 7, 8, 11, 14, 17, 22

Other Problems

- Appendix A: 1, 7, 10, 13, 14, 15, 19, 21, 30, 31, 34
- Appendix B: 3, 5, 8, 10, 12
- Chapter 2: 3, 4, 5, 6, 12, 13, 18, 19, 20